Appl. No. 10/785,522 Amdt. dated 10/12/2005 Response to Office Action of 08/24/2005 Attorney Docket No.: N1085-90179 TSMC 2002-0115

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

- 1 1. (Withdrawn) A floating gate memory array, comprising:
- a) an array of floating gate memory cells,
- b) a source line coupled to cells in a row of said array,
- c) a word line coupled to control gates of transistors of said memory cells in the row of said array,
- d) a read bit line and a program bit line connecting between said memory cells in each column of said array.
- 1 2. (Withdrawn) The memory array of claim 1, wherein said word line for the row of
- 2 memory cells in said array is segmented and each segment is driven by a word line
- 3 driver to allow simultaneous memory operations on a number of cells fewer in quantity
- 4 than that of a complete row.
- 1 3. (Withdrawn) The memory array of claim 1, wherein each row of memory cells in
- 2 said array is coupled to a unique source line.
- 1 4. (Withdrawn) The memory array of claim 3, wherein said read bit line and said
- 2 program bit line are merged into one bit line connecting between memory cells in a
- 3 column.
- 1 5. (Withdrawn) The memory array of claim 1, further comprising:
- a) a split gate read transistor and a split gate program transistor forming said
- 3 memory cells,

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- b) a floating gate of said read transistor connected to the floating gate of said program transistor and thereby merging the two floating gates,
- 6 c) said read bit line connected to a drain of the read transistor,
- 7 d) said program bit line connected to the drain of the program transistor.
- 6. (Withdrawn) The memory array of claim 5, wherein said program transistor is
 2 given an extra implant to increase threshold voltage to prevent punch-through.
- 1 7. (Withdrawn) The memory array of claim 1, further comprising:
- a) a split gate read transistor, a split gate program transistor and a spare split
 gate transistor forming said memory cells,
- b) a floating gate of said read transistor connected to the floating gate of said program transistor and thereby merging the two floating gates,
- 6 c) said read bit line connected to a drain of the read transistor,
- 7 d) said program bit line formed by a first program bit line and a second program 8 bit line.
- e) said first program bit line connected to the drain of the split gate program to transistor,
- 1) said second program bit line connected to the drain of the spare split gate transistor.
 - 1 8. (Withdrawn) The memory array of claim 7, wherein said memory cell in an
- 2 adjacent row of a column is formed with the first program bit line connected to the drain
- 3 of the spare split gate transistor and the second program bit line connected to the drain
- 4 of the split gate program transistor.

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- 1 9. (Withdrawn) The memory array claim 7, wherein said program transistor, said
- 2 read transistor and said spare transistor are formed with a thin cell.
- 1 10. (Withdrawn) The memory array of claim 7, wherein said memory cells are
- 2 formed with said split gate read transistor and said split gate program transistor,
- 3 whereby the first program bit line is connected to the drain of said program transistor
- 4 and the second program bit line is connected to the program transistor in said memory
- 5 cell of an adjacent row of the column.
- 1 11. (Withdrawn) The memory array of claim 10, wherein said program transistor is
- 2 formed with a thin cell and said read transistor is formed with a fat cell.
- 1 12. (Withdrawn) A method for re-write if disturbed, comprising:
- a) loading input address and data into a page buffer,
- 3 b) reading out original data from an address location of an array to a page
- 4 buffer,
- 5 c) erasing said address location, verifying the erasing of said address location,
- 6 and erasing bytes failing verification,
- 7 d) programming said address location, verifying the programming of said
- 8 address location, programming bytes failing programming,
- e) verifying data in unchanged portion of said address location
- 10 f) ending if verification of unchanged portion of said address location is passed,
- 11 else re-write failed locations.
- 1 13. (Withdrawn) The method of claim 12, wherein verifying the erasing of said
- 2 address location uses a verification read of a marginal "1".

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- (Withdrawn) The method of claim 12, wherein verifying the programming of said 1 14.
- address location uses a verification read of a marginal "0". 2
- (Previously Presented) A memory array utilizing cells with one split gate 1 15.
- transistor, comprising: 2
- an array of one transistor split gate cells arranged into rows and columns in 3
- which even addressed cells are located in a first row of cells and odd addressed cells 4
- are located in a second row of cells, 5
- a split source line connected to said even and odd addressed cells, 6
- said first row being connected with a first word line and said second row being 7
- 8 connected with a second word line, and
- said cells in one of said columns being connected to a bit line. 9
- (Previously Presented) The memory array of claim 15, wherein said row of even 1
- addressed cells is connected to a first source line and said row of odd addressed cells 2
- is connected to a second source line. 3
- (Currently Amended) The memory array of claim 15, wherein said first and 1 17.
- second-rows are connected with said first and second-word lines by segmenting each of 2
- said first and second word lines is divided into word line segments. 3
- (Currently Amended) The memory array of claim 17, wherein each word line 1 18.
- segment is driven with [[a]] an associated word line driver where and each word line 2
- segment is shorter in length than said row. 3
- (Previously Presented) A memory array utilizing cells with two split gate 1 19.
- 2 transistors, comprising:

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- an array of two transistor split gate cells arranged into rows and columns in which even addressed cells are located in a first row of cells and odd addressed cells are
- 5 located in a second row of cells,
- a split source line connected to said even and odd addressed cells,
- said first row being connected with a first word line and said second row being connected with a second word line, and
- 9 said cells in one of said columns being connected to a program bit line and a 10 read bit line.
- 1 20. (Previously Presented) The memory array of claim 19, wherein the two transistor
- 2 split gate cells comprise a first floating gate of a first split gate transistor coupled with a
- 3 second floating gate of a second split gate transistor.
- 1 21. (Previously Presented) The memory array of claim 19, wherein said row of even
- 2 addressed cells is connected to a first source line, and said row of odd addressed cells
- 3 is connected to a second source line.
- 1 22. (Currently Amended) The memory array of claim 19, wherein said first and
- 2 second rows are connected with said first and second word lines by segmenting each of
- 3 said first and second word lines is divided into word line segments.
- 1 23. (Currently Amended) The memory array of claim 22, wherein each word line
- 2 segment is driven with [[a]] an associated word line driver where and each word line
- 3 segment is shorter in length than said row.
- 1 24. (Previously Presented) A memory array utilizing cells with three split gate
- 2 transistors, comprising:

Attorney Docket No.: N1085-90179 Appl. No. 10/785,522 TSMC 2002-0115 Amdt. dated ___/__/. Response to Office Action of 08/24/2005 an array of cells containing three split gate transistors arranged into rows and 3 columns in which even addressed cells are located in a first row of cells and odd 4 addressed cells are located in a second row of cells. 5 a floating gate shared between a first and a second split gate transistor of said 6 7 three split gate transistors, a source line shared between said even and odd addressed cells, 8 said first row being connected with a first word line and said second row being 9 connected with a second word line, and 10 said cells in one of said columns being connected with a first program bit line, a 11 second program bit line and a read bit line. 12 (Previously Presented) The memory array of claim 24, wherein: 1 25. a) a first cell in a first row of one of the columns includes said first transistor, said 2 second transistor and a third transistor, 3 b) a second cell in a second row of said column includes said first transistor. 4 said second transistor, and said third transistor, 5 c) said first program bit line is connected to said first transistor in said first row 6 7 and said third transistor in said second row, d) said second program bit line is connected to said third transistor in said first 8 9 row and said first transistor in said second row, and

e) said read bit line is connected to said second transistor of said first row and to

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said second transistor of said second row.

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- 1 26. (Previously Presented) The memory аггау of claim 24, wherein said first and
- 2 second rows are connected with said first and second word lines by segmenting said
- 3 first and second word lines.
- 1 27. (Original) The memory array of claim 26, wherein each word line segment is
- 2 driven with a word line driver where each segment is shorter in length than said row.
- 1 28. (Original) The memory array of claim 26, wherein said first, second and third
- 2 transistors are thin transistors.
- 1 29. (Previously Presented) A memory аггау utilizing cells with two split gate
- 2 transistors, comprising:
- an array of cells containing two split gate transistors arranged into rows and
- 4 columns in which even addressed cells are located in a first row of cells and odd
- 5 addressed cells are located in a second row of cells,
- a floating gate shared between a first and a second split gate transistor of said two split gate transistors,
- 8 a source line shared between said even and odd addressed cells,
- 9 said first row being connected with a first word line and said second row being
- 10 connected with a second word line,
- said cells in one of said columns being connected with a first program bit line, a
- 12 second program bit line and a read bit line.
 - 1 30. (Previously Presented) The memory array of claim 29, wherein:
- a) a first cell in a first row of one of said columns includes said first transistor and
- 3 said second transistor,

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- b) a second cell in a second row of said column includes said first transistor and said second transistor,
- 6 c) said first program bit line is connected to said first transistor in said first row,
- 7 d) said second program bit line is connected to said first transistor in said 8 second row.
- e) said read bit line is connected to said second transistor of said first row and to said second transistor of said second row.
- 1 31. (Previously Presented) The memory array of claim 29, wherein said first and
- 2 second rows are connected with said first and second word lines by segmenting said
- 3 first and second word lines.
- 1 32. (Original) The memory array of claim 31, wherein each word line segment is
- 2 driven with a word line driver where each segment is shorter in length than said row.
- 1 33. (Original) The memory array of claim 31, wherein said first transistor is a thin
- 2 transistor and said second transistor is a fat transistor.
- 1 34. (Previously Presented) A memory array containing cells with two split gate
- 2 transistors, comprising:
- an array of cells containing two split gate transistors arranged in rows and
- 4 columns,
- a floating gate shared between a first and a second split gate transistor of said
- 6 two split gate transistors,
- 7 means for increasing the threshold voltage of said first split gate transistor,
- 8 a source line shared between said even and odd addressed cells,

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- said first row being connected with a first word line and said second row being
 connected with a second word line.
- said cells in one of said columns being connected with a program bit line and a read bit line.
 - 1 35. (Original) The memory array of claim 34, wherein the means for increasing the
- 2 threshold voltage of said first split gate transistor uses an added implantation.
- 1 36. (Original) The memory array of claim 34, wherein the means for connecting
- 2 between cells in a column further comprising:
- a) a first cell in a first row of a column containing said first transistor and said
 second transistor,
- 5 · b) a second cell in a second row of said column containing said first transistor 6 and said second transistor.
- 7 c) said program bit line connecting to said first transistor in said first row and 8 said second row,
- 9 d) said read bit line connecting to said second transistor of said first row and to said second transistor of said second row.
- 1 37. (Currently Amended) The memory array of claim 34, wherein the means for
- 2 connecting said first and second rows with said first and second word lines is done by
- 3 segmenting each of said first and second word lines is divided into word line segments.
- 1 38. (Currently Amended) The memory array of claim 37, wherein each word line
- 2 segment is driven with [[a]] an associated word line driver where and each word line
- 3 segment is shorter in length than said row.
- 1 39. (Withdrawn) A method for re-writing disturbed cells, comprising:

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- a) a means for loading a page buffer with input addresses and data,
- 3 b) a means for reading data from a memory location into said page buffer,
- c) a means for erasing said address location and re-erasing those bytes failing verification of said erasing,
- d) a means for programming said memory location and re-programming those bytes failing verification of said programming,
- e) a means for verifying data in unchanged portion of said memory location and
 ending process if verification is true, else return to step c) to re-program data.
- 1 40. (Withdrawn) The method of claim 39, wherein verification of said erasing uses a read for a marginal "1".
- 1 41. (Withdrawn) The method of claim 39, wherein verification of said programming uses a read of for a marginal "0".